LESSION PLAN

NAME OF THE FACULTY : RAVINDER KUMAR

DISCIPLINE : ECE

SEMESTER : FOURTH

SUBJECT : DE-II

LESSON PLAN DURATION : - 15 weeks (from January 2018 to April 2018)

WORK LOAD (LECTURE/PRACTICAL) PER WEEK (IN HOURS):- LECTURE-**03**, PRACTIACL-**03**

WEEK	THEORY		PRACTICAL	
	LECTURE DAY	TOPIC (including assignment/test)	PRACTICAL DAY	TOPIC
1st	1st	Logic family classification- TTL, ECL, MOS, CMOS	1st Group-1	Verify the operation of D/A converter
	2nd	Types of integration- SSI, MSI, LSI, VLSI Characteristics of TTL and CMOS and comparison		
	3rd	Propagation delay, speed, noise margin, logic level power dissipation	2nd Group-2	Verify the operation of D/A converter
2nd	4th	Fan in, fan out, power supply requirements, open collector and totem pole output circuits.	3rd Group-1	Verify the operation of A/D converter
	5th	Operation of standard TTK and CMOS. NAND, NOR gates.		
	6th	CMOS to TTL interfacing and TTL to CMOS interfacing. Assignment-1	4th Group-2	Verify the operation of A/D converter
3rd	7th	Introduction to tri state devices. Tristate buffer and inverter circuits	5th Group-1	Verify the writing and reading of RAM IC
	8th	Test Logic family		
	9th	D/A converters Performance , characteristics of D/A converter.	6th Group-2	Verify the writing and reading of RAM IC
4th	10th	Binary register network Applications	7th Group-1	Design JK flip flop counter and verify truth table
	11th	Resistance ladder network method of D/A converters. Applications		
	12th	A/D converters Performance, characteristics of A/D converters.	8th Group-2	Design JK flip flop counter and verify truth table

5th	13th	Single Slope, Dual Slope	9th Group-1	Familiarity with the use of EPROM programs and UV index
	14th	Successive approximation A/D converter		
	15th	Parallel A/D converters	10th Group-2	Familiarity with the use of EPROM programs and UV index
6th	16th	Memory organization. Classification of semiconductor memories.	11th Group-1	**Revision**
	17th	ROM, PROM, DROM		
	18th	EPROM, EEPROM, RAM, RAM Expansion of memory	12th Group-2	**Revision**
7th	19th	Assignment	13th Group-1	Exercise on programming of EPROM
	20th	**1st Sessional Test**		
	21th	CCD memories	14th Group-1	Exercise on programming of EPROM
8th	22th	Content Addressable memory	15th Group-1	**Revision**
	23th	Programmable logic devices		
	24th	PROM at PLD Assignment	16th Group-2	**Revision**
9th	25th	Programmable logic array (PLA) Programmable array logic (PAL) Difference between PLA and PAL	17th Group-1	Design and implementation of full adder and full subtractor
	26th	Field Programmable Gate Array (FPGA)		
	27th	Familiarization with ICs	18th Group-2	Design and implementation of full adder and full subtractor
10th	28th	Combinational circuits	19th Group-1	**Revision**
	29th	Minimization of Boolean expression using Quine Mcclaskey method		
	30th	Minimization of Boolean expression using Quine Mcclaskey method	20th Group-2	**Revision**
11th	31th	Sequential Circuits Essential components of sequential circuits Assignment	21th Group-1	Verify the logical operation, arithmetic operation of binary numbers using IC 74181
	32th	Synchronous and asynchronous circuits		
	33th	Sequential circuits, Classification of sequential circuits	22th Group-2	Verify the logical operation, arithmetic operation of binary numbers using IC 74181

12th	34th	Meely and Moore machine	23th Group-1	Revision & Viva
	35th	Counters		
	36th	Design of counters using JK flip flop	24th Group-2	Revision & Viva
13th	37th	Assignment	25th Group-1	Revision & Viva
	38th	Revision		
	39th	**2nd Sessional Test**	26th Group-2	Revision & Viva
14th	40th	Basic idea about Arithmetic Logic Unit wrt IC 74181 and applications	27th Group-1	Revision & Viva
	41th	Implementation of binary multiplication and division, Implementation of binary addition and subtraction		
	42th	Fuzzy sets and their operations, Classical sets and their operations, Fuzzy relations Properties of membership functions	28th Group-2	Revision & Viva
15th	43th	Fuzzy relations Properties of membership functions	29th Group-1	Revision & Viva
	44th	Fuzzification, Defuzzification, Fuzzycontrol system Assignment		
	45th	**3rd Sessional Test**	30th Group-2	Revision & Viva