NAME OF THE FACULTY : RAVINDER KUMAR

DISCIPLINE : ECE

SEMESTER : 3rd

SUBJECT : DIGITAL ELECTRONICS

LESSON PLAN DURATION : - 15 weeks (from July- 2018 to Dec- 2018)

WORK LOAD (LECTURE/PRACTICAL) PER WEEK (IN HOURS):- LECTURE-**03**, PRACTIACL-**03** PER GROUP

WEEK	THEORY		PRACTICAL		
	Lecture / Hrs	TOPIC (Including Assignment/Test)	Practical / Hrs		Experiment
1st	1	**Introduction to Digital Electronics:** Distinction between analog and digital signal.	Group-1	1	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates
				2	
	2	Applications and advantages of digital signals.		3	
			Group-2	1	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates
	3	**Number System:** Binary, octal and hexadecimal number system		2	
				3	
2nd	4	Conversion from decimal and hexadecimal to binary and vice-versa.	Group-1	1	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates
				2	
	5	Binary addition and subtraction including binary points. 1's and 2's complement method of addition/ subtraction		3	
			Group-2	1	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates
	6	**Codes and Parity:** Concept of code, weighted and non-weighted codes		2	
				3	
3rd	7	Examples of 8421, BCD, excess-3 and Gray code	Group-1	1	Realisation of logic functions with the help of NAND or NOR gates
				2	
	8	Concept of parity, single and double parity and error detection		3	
			Group-2	1	Realisation of logic functions with the help of NAND or NOR gates
	9	**Logic Gates and Families:** Concept of negative and positive logic.		2	
				3	
4th	10	Definition, symbols and truth tables of NOT, AND, OR Gates	Group-1	1	To design a half adder using XOR and NAND gates and verification of its operation
				2	
	11	Definition, symbols and truth tables of NAND, NOR, EXOR Gates		3	
			Group-2	1	To design a half adder using XOR and NAND gates and verification of its operation
	12	Definition, symbols and truth tables of NAND and NOR as universal gates.		2	
				3	

5th	13	Introduction to TTL and CMOS logic families	Group-1	1 2 3	Construction of a full adder circuit using XOR and NAND gates and verify its operation
	14	**Assignment-1**			
	15	**Sessional Test-1**	Group-2	1 2 3	Construction of a full adder circuit using XOR and NAND gates and verify its operation
6th	16	**Logic Simplification:** Postulates of Boolean algebra, De Morgan's Theorems	Group-1	1 2 3	Revision Experiment Performed
	17	Implementation of Boolean (logic) equation with gates			
	18	Karnaugh map (upto 4 variables)	Group-2	1 2 3	Revision Experiment Performed
7th	19	Simple application in developing combinational logic circuits	Group-1	1 2 3	Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops
	20	**Arithmetic circuits:** Half adder and Full adder circuit			
	21	Half adder and Full adder circuit, design and implementation	Group-2	1 2 3	Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops
8th	22	**Decoders, Multiplexeres, Multiplexeres and Encoder:** Introduction	Group-1	1 2 3	Verification of truth table for encoder and decoder ICs, Mux and DeMux
	23	Four bit decoder circuits for 7 segment display and decoder/driver ICs			
	24	Basic functions and block diagram of MUX and DEMUX with different ICs	Group-2	1 2 3	Verification of truth table for encoder and decoder ICs, Mux and DeMux
9th	25	Basic functions and block diagram of Encoder	Group-1	1 2 3	To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation
	26	**Latches and flip flops:** Concept and types of latch with their working and applications			
	27	Operation using waveforms and truth tables of RS, T, D, Master/Slave JK flip flops.	Group-2	1 2 3	To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation
10th	28	Difference between a latch and a flip flop.	Group-1	1 2 3	Revision Experiment Performed
	29	**Assignment-2**			
	30	**Sessional Test-2**	Group-2	1 2 3	Revision Experiment Performed

11th	31	**Counters:** Introduction	Group-1	1 2 3	To design a 4 bit ring counter and verify its operation
	32	Introduction to Asynchronous counters	Group-2	1 2 3	To design a 4 bit ring counter and verify its operation
	33	Introduction to Synchronous counters			
12th	34	Binary counters	Group-1	1 2 3	Use of Asynchronous Counter ICs (7490 or 7493)
	35	Divide by N ripple counters			
	36	Decade counter, Ring counter	Group-2	1 2 3	Use of Asynchronous Counter ICs (7490 or 7493)
13th	37	**Shift Register:** Introduction and basic concepts including shift left and shift right. Serial in parallel out, serial in serial out	Group-1	1 2 3	Revision Experiment Performed
	38	Parallel in serial out, parallel in parallel out. Universal shift register.			
	39	**A/D and D/A Converters:** Working principle of A/D and D/A converters, Stair step Ramp A/D converter, Dual Slope A/D converter.	Group-2	1 2 3	Revision Experiment Performed
14th	40	Successive Approximation A/D Converter, detail study of : Binary Weighted D/A converter, R/2R ladder D/A converter. Applications of A/D and D/A converter	Group-1	1 2 3	Revision Experiment Performed
	41	**Semiconductor Memories:** Memory organization, classification of Semiconductor memories			
	42	(RAM, ROM, PROM, EPROM, EEPROM), static and dynamic RAM	Group-2	1 2 3	Revision Experiment Performed
15th	43	Introduction to 74181 ALU IC	Group-1	1 2 3	Revision Experiment Performed
	44	**Assignment- 3**			
	45	**Sessional Test- 3**	Group-2	1 2 3	Revision Experiment Performed